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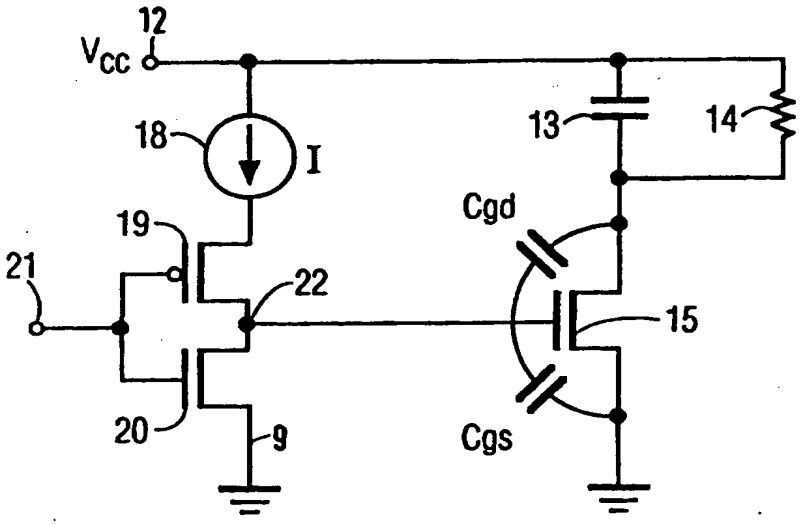

(57) Abstract

An active current limiting circuit in which a semiconductor power transistor (15) is turned on slowly by charging its gate-source capacitance slowly, preferably by applying a ramp-type drive waveform to the gate of the power transistor (15). The slow turn-on of the power transistor (15) automatically limits the amplitude of the current flow through the main current path of the power transistor (15). In addition, ringing in the circuit is eliminated by the slow turn-off of the power transistor (15).

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Pre-regulator with active current limiting for power transistor

BACKGROUND OF THE INVENTION

This invention relates to power supply circuits and, more particularly, to a power supply pre-regulator circuit of the switching type which provides a current limiting characteristic for the switching power transistor.

In order to prevent damage to the power transistor and other circuit components in a switching type power supply pre-regulator circuit, it is common practice to connect a high wattage resistor of approximately 10 ohms, for example, in series circuit with the switching power transistor. This, of course, wastes a significant amount of power and is to be avoided whenever possible. Furthermore, a high wattage resistor is both bulky and expensive and thus raises the overall cost of any circuit of which it is a part.

The problem of limiting the current in a power transistor in the case where the load circuit includes a significant capacitance component or the power transistor itself exhibits a substantial inherent inter-electrode capacitance is particularly vexing.

One possible solution to the problem of limiting the load capacitor charging current and hence the current through the power transistor is disclosed in U.S. patent No. 5,469,046, and which is hereby incorporated by reference. In that patent, the load capacitor charging current is reduced while the power dissipation is kept to a minimum by means of a control technique in which the load capacitor is charged twice in each half cycle of the AC supply voltage, that is both on the leading edge and the trailing edge of the full-wave rectified supply voltage applied to the load capacitor via the switching power transistor. Although the pre-regulator power supply circuit described therein achieved its objects, it did so at the cost of a slight amount of additional circuit complexity and therefore extra integrated circuit silicon chip area.

In U.S. patent 4,954,917 there is described a short circuit protection scheme for a driver circuit power transistor. Short-circuit protection is provided in this patent by sensing the saturation condition of the power transistor and when a short-circuit condition is sensed, the drive circuit reduces the gate voltage drive thereby limiting the current that can flow through the power transistor. This is achieved by changing the gate voltage from one reference voltage level to another reference voltage level. This patent does not address the

problem of limiting the current at start-up in a power supply pre-regulator circuit and also when the load capacitor is charged during each supply cycle of the AC supply voltage for the circuit.

SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide an improved pre-regulator circuit having a current limiting capability at start-up of the circuit and when the load capacitor is charged at the beginning of each supply voltage cycle.

Another object of the invention is to simplify the control and reduce the silicon chip area required for a pre-regulator power supply integrated circuit.

A further object of the invention is to provide an inexpensive power supply with active current limiting for the power transistor of the pre-regulator circuit.

The foregoing and other objects of the invention are achieved by means of a power supply pre-regulator circuit which actively limits the current in the switching power transistor by providing a slow turn-on of this transistor by charging its inherent gate capacitance with a fixed low current.

Current limiting is provided in the pre-regulator current limiting circuit by continuously changing the gate voltage of the power transistor by applying a ramp voltage to its gate electrode, rather than the conventional square wave gate drive voltage of prior art circuits.

The ramp voltage is generated by charging a capacitor using a current source. The power transistor device in the pre-regulator circuit is turned on at the beginning of each supply cycle when the voltage across the power transistor, V_{ds}, is close to zero. As the gate of the power transistor is charged slowly, the current flowing in the power transistor, I_d, also increases slowly. However, the supply voltage is increasing during this time which causes an increase in the voltage V_{ds}. As a result, the power transistor operates in the constant current region of the power transistor and the power transistor acts like a voltage controlled current source having a current limiting characteristic. The controlling voltage is the gate voltage and the controlled current is the drain or collector current, I_d. During turn-on of the power transistor, the drain current versus drain voltage characteristic follows a curved concave path instead of the linear path that occurs when a square wave gate drive voltage is utilized.

As a result of the slow turn-on of the power transistor by slowly charging its gate capacitance, the power transistor acts like a voltage controlled current source in which the gate voltage is the control voltage. Current limiting thus is achieved by slowly increasing

the power transistor current by the slow control of its gate voltage.

The present invention can be used in the pre-regulator power supply circuit described in the above-mentioned co-pending U.S. application and which is modified slightly to charge the load capacitor only once in each rectified half cycle of the AC supply voltage.

BRIEF DESCRIPTION OF THE DRAWING

The invention will now be described in greater detail with reference to the accompanying drawing, in which:

Fig. 1 is a diagram illustrating the basic concept of the invention,

Figs. 2A-2C are waveforms of a prior art square wave type drive circuit,

Figs. 3A-3C are waveforms illustrating the reduced peak drain current obtained by means of the invention,

Fig. 4 is a simplified diagram of a circuit for deriving a ramp gate drive waveform for the power transistor, and

Fig. 5 is a detailed circuit diagram of an embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 shows a simplified circuit diagram which illustrates the novel active current limiting concept underlying the present invention. A source of AC supply voltage 10 of, for example, 115 V, 60 Hz, has a pair of output terminals coupled to the input terminals of a full wave diode rectifier bridge circuit 11 having a positive DC output terminal 12 coupled to first terminals of a load capacitor 13 and a load 14, the latter shown as a resistor in the interest of simplicity.

The second terminals of the load capacitor 13 and load resistor 14 are connected in common to a first main electrode (drain) of a semiconductor power transistor 15, for example, a Lateral Insulated Gate Bipolar Transistor (LIGBT) with its source electrode connected to the low (negative) DC output terminal 9 of the bridge rectifier circuit 11.

A control circuit 16 applies a switching control voltage to the control electrode (gate) of the power transistor 15 to switch it on and off and thereby control the supply of current to the load 14 and the load capacitor 13 from the pulsatory DC supply voltage at the output of the bridge rectifier circuit 11. The control circuit 16 and the power transistor 15 may be part of a power integrated circuit illustrated diagrammatically by means of a dashed line rectangular box 17. The bridge rectifier circuit 11, the load 14 and the load capacitor 13

are off-chip components of the pre-regulator power integrated circuit.

The circuit shown in Fig. 1 will provide current limiting at start-up of the pre-regulator circuit and when the load capacitor 13 is charged at the beginning of each periodic supply voltage cycle. At start-up, the load capacitor 13 is discharged. As a result, a large current will initially flow from the voltage source 11 to charge the load capacitor 13. If this current is not limited, it can damage the semiconductor power transistor (LIGBT) 15. In addition, the load capacitor 13 will be charged during each cycle of the pulsatory DC supply voltage so as to replenish the charge depleted from the load capacitor by the load 14. At this time, a large peak current can flow from the voltage supply circuit and it is desirable to limit its peak value.

According to the present invention, current limiting is provided for the pre-regulator circuit by continuously charging the power transistor gate voltage by applying a ramp voltage to the gate electrode rather than the conventional square wave gate drive voltage. The ramp voltage may be generated by charging a capacitor using a current source. The power transistor 15 in the pre-regulator circuit is turned on at the beginning of each supply cycle when the drain-source voltage V_{ds} of the power transistor 15 is close to zero. As the gate of the power transistor 15 is charged slowly, the drain current I_d flowing in the power transistor increases slowly. However, the supply voltage is increasing during this time which causes an increase in the voltage V_{ds}. Therefore, the power transistor 15 is forced to operate in the constant current region of its characteristic so that the power transistor 15 acts like a voltage controlled current source providing a current limiting action.

The controlling voltage is the gate voltage and the controlled current is the drain current, I_d. The drain current versus drain voltage characteristic thus follows a concave upward path during turn-on of the power transistor 15. This is in contrast to the linear path followed during turn-on of a power transistor when a square wave gate drive waveform is used. The drain-source voltage, V_{ds}, is low at all times and therefore switching losses are low.

As mentioned above, the slow turn-on of the power transistor is achieved by slowly charging its gate capacitance by using a ramp gate drive voltage so that the power transistor acts like a voltage controlled current source in which the control voltage is the gate voltage. Thus, by increasing the power transistor current slowly by controlling its gate voltage, current limiting can be achieved. However, this approach to power transistor turn-on leads to an increase in switching losses as the device enters the saturation region where both the drain current and the drain-source voltage of the power transistor are high. However, due

to the low frequency of operation, this increase in switching losses is not a serious drawback.

Figs. 2A, 2B and 2C show the waveforms of the power transistor gate voltage V_{gs}, drain current I_d and drain-source voltage V_{ds}, respectively, for a power transistor driven with a square wave type gate voltage. As can be seen from the drain current waveform of Fig. 2B, the peak drain current reaches a fairly high value in the case of a conventional square wave gate voltage drive circuit. In contrast, Figs. 3A, 3B and 3C show the corresponding gate voltage, drain current and drain-source voltage waveforms, respectively, for a circuit in accordance with the invention of Fig. 1. Fig. 3B clearly indicates the lower peak drain current that is achieved in accordance with the present invention.

Fig. 4 shows an example of a simplified control circuit 16 which can be used to drive the gate of the semiconductor switching power transistor 15 in the circuit of Fig. 1. The drive circuit consists of a constant current source 18 connected in series circuit with a first P-type field effect transistor 19 and a second N-type field effect transistor 20 between a DC supply voltage, V_{cc}, and ground. The gate electrodes of the transistors 19 and 20 are connected in common to a control input terminal 21 and the common junction 22 between the transistors 19 and 20 is connected to the gate of the switching power transistor 15. The power transistor 15, for example, a LIGBT power transistor, is connected in another series circuit with a parallel circuit of the load capacitor 13 and the load 14 between the DC supply voltage, V_{cc}, and ground. The gate-drain capacitance Cgd and the gate-source capacitance Cgs of the power transistor 15 also are shown.

When the control voltage applied to input terminal 21 goes low, the field effect transistor 19 turns on and the constant current source 18 supplies a charge current to the gate-source capacitance Cgs of power transistor 15, which produces a ramp-like voltage at the gate electrode so that the power transistor 15 is turned on at a relatively slow rate. When the control voltage at input terminal 21 goes high, transistor 19 turns off and transistor 20 turns on so as to discharge, via the ground line, the voltage accumulated on the gate-source capacitance Cgs. In this way, the slow turn on of the power transistor 15 is accomplished so as to achieve the objects of the present invention. If the value of the gate-source capacitance Cgs is insufficient, it is possible to connect a further capacitor between the gate and source of power transistor 15. The same is true for the gate-drain capacitance Cgd of transistor 15.

Fig. 5 shows a practical circuit implementation of the slow turn on driver circuit of the invention. The circuit shown also has a provision for slow turn-off of power transistor. A first series circuit consisting of a N-type field effect transistor M1 and a P-type filed effect transistor M2 is connected between a source of positive DC supply voltage, V_{cc}

and ground.

A second series circuit consisting of a P-type field effect transistor M3 and a N-type field effect transistor M6 is connected between the DC supply voltage V_{cc} and ground and a third series circuit consisting of P-type field effect transistors M4 and M7, and N-type field effect transistors M8 and M5 also is connected between the DC voltage V_{cc} and ground.

The gate and drain of transistor M2 are connected together and to the gate of transistor M3 and to the gate of transistor M4. The gate of transistor M6 is connected to a control voltage input terminal 22. A bias voltage terminal 23 is connected to the gates of transistors M1 and M5. The gate electrodes of transistors M7 and M8 are connected together and to a common junction point between transistors M3 and M6. The output is taken from an output terminal 24 at the common junction point of the transistors M7 and M8.

The basis for the improved operation of the slow turn on/turn off driver circuit lies in controlling the drain current through the gate drive waveform, and thereby limiting the current when the power transistor switches on and in addition reducing any RLC ringing, caused by an inductive component in the load, when it switches off. As the power transistor switches off, the gate voltage falls and discharges the gate to source and gate to drain capacitances and reduces the current through the power transistor to zero. However, the current through the inductive component cannot fall to zero immediately. This causes voltage ringing (oscillation) in prior art driver circuits.

The slower turn-on and turn-off time of the present driver circuit eliminates any tendency toward RLC oscillation in the circuit as the current in the inductive component is allowed to drop to zero, in addition to the current limiting feature previously discussed.

Transistors M1, M2, M3, M4 and M5 are used to set up a bias current based on a bias signal from the bias voltage terminal 23. When the input 22 goes high, transistor M6 turns on, which turns transistor M7 on as well and the output 24 is pulled high. When the input goes low, transistor M6 turns off and transistor M8 turns on, and the output 24 is pulled low. Current through transistors M7 and M8 is fixed by the bias voltage at bias voltage terminal 23. However, the turn on/turn off rate can be controlled or adjusted by applying suitable voltages to the common junction point 25 of the transistors M4 and M7 and the common junction point 26 of the transistors M8 and M5, respectively, thereby to provide external control of the on/off currents. Thus, the charge and discharge of the power transistor parasitic capacitance can be controlled to limit the current and to limit any RLC ringing in the circuit.

Although the invention has been described in connection with a preferred

embodiment thereof, it will be apparent to those skilled in the art that various changes and modifications can be made without departing from the true spirit and scope of the invention as defined in the appended claims.

CLAIMS:

1. An active current limiter circuit for a switchable power transistor (15) comprising:

first (12) and second (9) input terminals for supplying a DC supply voltage to the circuit,

means for coupling a load circuit (13, 14) and the switchable power transistor (15) to said first (12) and second (9) input terminals so that the power transistor (15) controls the flow of current from said input terminals (12, 9) to the load circuit (13, 14), and

a control circuit (16) coupled to a control electrode of the power transistor (15) for switching the power transistor (15) on and off, wherein said control circuit (16) supplies a control signal to said control electrode having a waveform that produces a relatively slow turn-on of the power transistor (15) sufficient to limit the rate of current flow through the main current path of the power transistor (15).

2. The active current limiter circuit as claimed in Claim 1 wherein said control circuit (16) includes means (18, 19) for applying a ramp-type voltage waveform to the control electrode of the power transistor (15).

3. The active current limiter circuit as claimed in Claim 2 wherein said means for applying a ramp-type voltage comprises:

a source of constant current (18),

a further input terminal (21) for a control voltage, and

switching means (19, 20) controlled by the control voltage at said further input terminal (21) for selectively coupling the control electrode of the power transistor (15) to said constant current source (18) and to a point of reference voltage (9).

4. The active current limiter circuit as claimed in Claim 3 wherein said switching means comprises;

first (19) and second (20) transistors connected in series circuit with said constant current source (18) across said first (12) and second (9) input terminals with their control electrodes connected in common to said further input terminal (21) and with a junction point (22) therebetween connected to the control electrode of the power transistor (15).

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5. The active current limiter circuit as claimed in Claim 2 wherein;

said coupling means connects the load circuit (13, 14) in series circuit with the power transistor (15) across the first (12) and second (9) input terminals, and

said power transistor (15) exhibits a finite gate-source capacitance (V_{gs}).

6. The active current limiter circuit as claimed in Claim 1 wherein the control circuit (16) includes a constant current source (18) and the power transistor (15) comprises a lateral insulated gate bipolar transistor with its source electrode connected to the second input terminal (9) and its gate electrode coupled to said constant current source (18) so that the gate-source capacitance of the power transistor (15) is slowly charged with a constant current so as to develop a ramp-type waveform at the gate of the power transistor (15).

7. The active current limiter circuit as claimed in Claim 1 wherein the control circuit (16) comprises:

a first series circuit including a diode-connected transistor (M2) and a first transistor (M1) connected between said first (12) and second (9) input terminals,

a second series circuit including second (M3) and third (M6) transistors connected between said first (12) and second (9) input terminals,

a third series circuit including fourth (M4), fifth (M7), sixth (M8) and seventh (M5) transistors connected between said first (12) and second (9) input terminals,

a control terminal (22) connected to a control electrode of the third transistor (M6),

first means coupling the diode-connected transistor (M2) to respective control electrodes of the second (M3) and fourth (M4) transistors,

a bias voltage terminal (23) connected in common to control electrodes of the first (M1) and seventh (M5) transistors,

second means coupling control electrodes of the fifth (M7) and sixth (M8) transistors in common to a junction point between the second (M3) and third (M6) transistors, and

an output terminal (24) coupled to a junction point between the fifth (M7) and sixth (M8) transistors.

8. The active current limiter circuit as claimed in Claim 7 wherein:

the second (M3) and third (M6) transistors are of opposite conductivity type,

the fourth (M4) and fifth (M7) transistors are of the same conductivity type and the sixth (M8) and seventh (M5) transistors are of opposite conductivity type to that of the fourth (M4) and fifth (M7) transistors.

9. The active current limiter circuit as claimed in Claim 7 further comprising:

a first control terminal (25) coupled to a junction point between the fourth (M4) and fifth (M7) transistors for adjusting the rate of turn-on current, and

a second control terminal (26) coupled to a junction point between the sixth (M8) and seventh (M5) transistors for adjusting the rate of turn-off current.

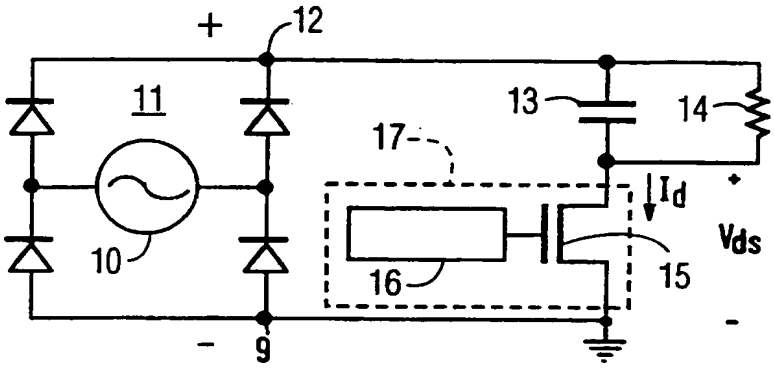
+
12
11
13
14
17
Id
Vds
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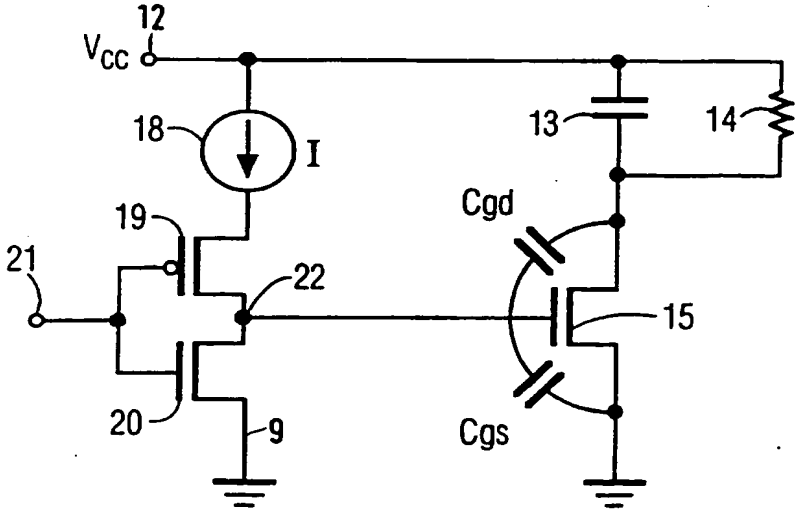
FIG. 1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Vcc
18
I
13
14
Cgd
19
21
22
15
20
9
Cgs

FIG. 4

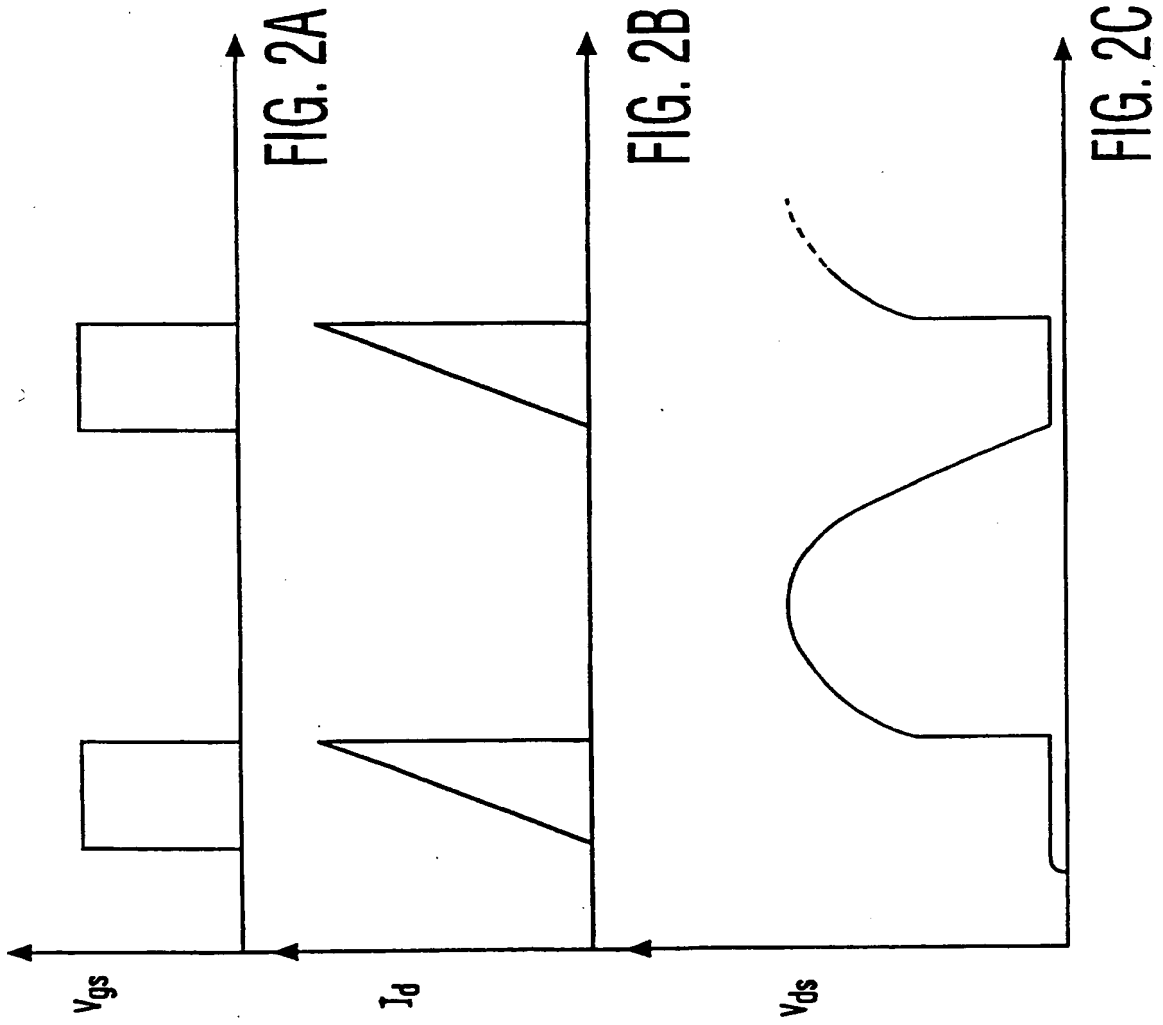
FIG. 2A
FIG. 2B
FIG. 2C
V_{gs}
I_d
V_{ds}

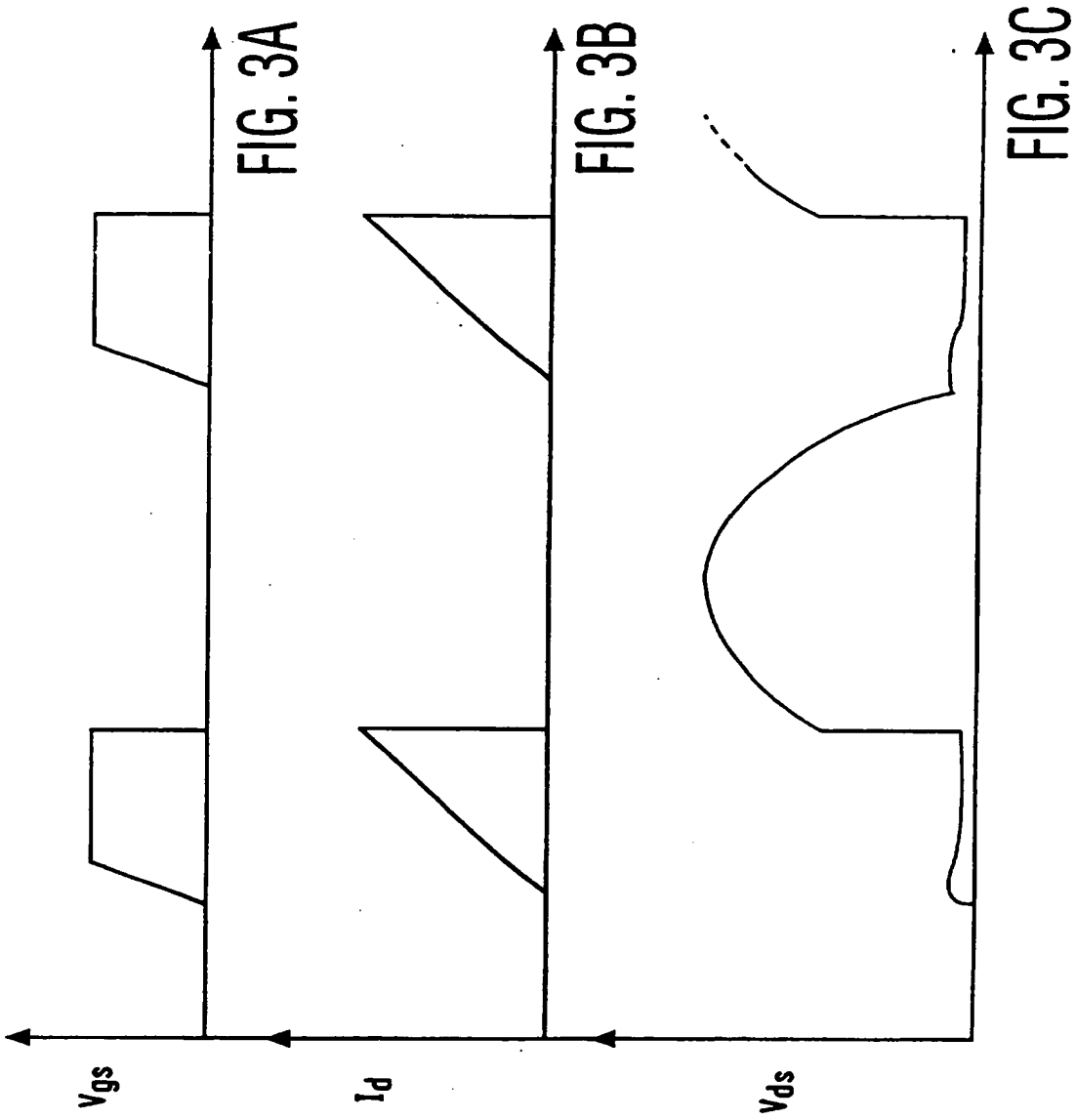
FIG. 3A
FIG. 3B
FIG. 3C
V_{gs}
I_d
V_{ds}

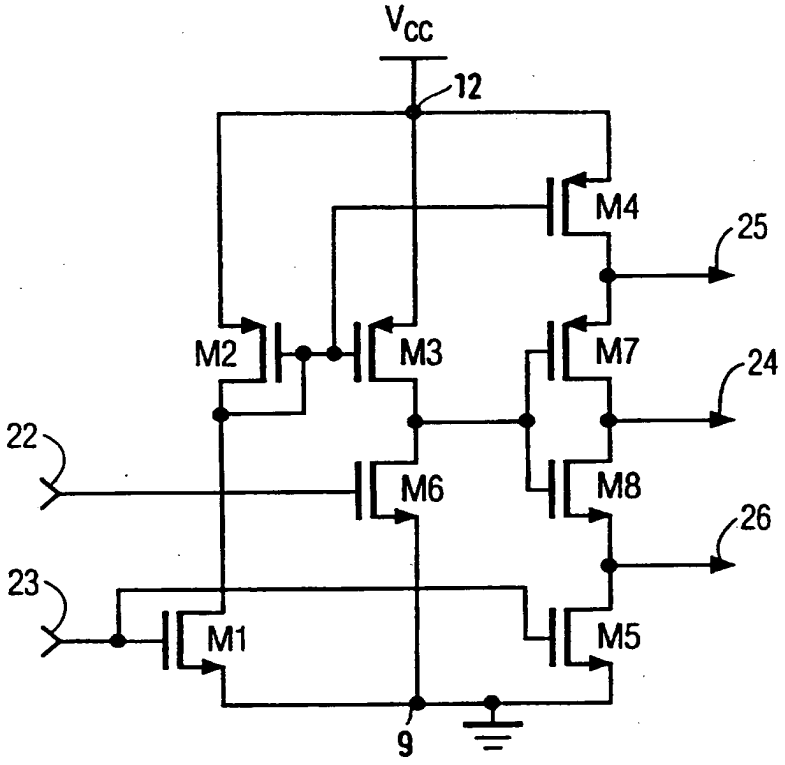

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB 96/00940

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H03K 17/08.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H03K, H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GB 2140996 A (GENERAL ELECTRIC COMPANY), 5 December 1984 (05.12.84), see the whole document	1-6
X	EP 0164615 A2 (INTERNATIONAL BUSINESS MACHINES CORPORATION), 18 December 1985 (18.12.85), page 5, line 15 - page 8, line 28	1
X	WO 9524076 A1 (APPLE COMPUTER, INC.), 8 Sept 1995 (08.09.95), page 4, line 20 - page 6, line 11	1,2
A	EP 0622889 A2 (PHILIPS ELECTRONICS N.V.), 2 November 1994 (02.11.94), abstract	1

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
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INTERNATIONAL SEARCH REPORT

Information on patent family members

03/02/97

International application No.
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		US-A- 5469046	21/11/95

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